REMARKS

Claims 59-84, 92 and 93 are pending in this application. Claim 59 has been amended. New claims 92 and 93 have been added to round out the scope of protection afforded by the invention.

Claims 59-65 and 67-84 stand rejected under 35 U.S.C. § 102 as being anticipated by Summerfelt et al. (U.S. Patent No. 5,612,574) ("Summerfelt"). This rejection is respectfully traversed.

The claimed invention relates to an integrated circuit structure obtained by a particular process methodology. As such, amended independent claim 59 recites an "integrated circuit substrate" formed by *inter alia* "placing said integrated circuit substrate into a reactive chamber; introducing into said chamber an etching gas" and "generating a plasma of said etching gas at a first power level and contacting said substrate with said first power level plasma for a first predetermined time." Amended independent claim 59 further recites that the integrated circuit substrate is formed by "generating a plasma of said etching gas at a second power level in said chamber and contacting said integrated circuit substrate with said second power level plasma for a second predetermined time, wherein said second power level plasma is a higher power plasma than said first power level plasma."

Summerfelt relates to a semiconductor structure "using high-dielectric-constant materials and an adhesion layer." (Abstract; Title). Summerfelt teaches that "an interlevel isolation layer" and a "barrier layer" are formed over the active region and "disposed outwardly from the conductive plug." (Col. 2, lines 42-46). "[A]n oxygen-stable inner electrode is formed outwardly from portions of the interlevel isolation layer and the barrier layer." (Col. 2, lines 46-48). Summerfelt also teaches that "[A]n adhesion layer is disposed between the oxygen-stable inner electrode and the interlevel isolation layer and the barrier layer." (Col. 2, lines 48-51). In this manner, "the problems of adhesion between the oxygen-stable layer and the interlayer isolation layer in devices including such materials" are eliminated. (Col. 2, lines 29-32).

At the outset, Applicant notes that courts have generally held that a product-by-process claim is a "perfectly acceptable one so long as the claims particularly point out and distinctly claim the product or genus of products for which protection is sought." *See* In re Brown, 459 F.2d 531, 535, 173 USPQ 685 (CCPA 1972). A product-by-process claim is allowed when the product cannot be adequately described in any other manner. *See* Bonito Boats Inc. v. Thunder Craft Boats Inc., 489 U.S. 141, 9 U.S.P.Q.2d 1847 (1989); In re Jochim, 11 U.S.P.Q.2d 1561, 1563 (Bd. Pat. App. & Int'f 1988). This way, "where one has produced an article . . . and where it is not possible to define the characteristics which make it inventive except by referring to the process by which the article is made, he (the applicant) is permitted to so claim his article, but is limited in his protection to articles produced by his method referred to in the claims." In re Moeller, 117 F.2d 565, 568, 48 U.S.P.Q. 542 (CCPA 1941); *See also* Scripps Clinic & Research Foundation v. Genentech Inc., 666 F. Supp. 1379, 3 U.S.P.Q.2d 1481 (N.D. Calif. 1987) ("A product-by-process claim is infringed only by a product produced by following the same process described in the claim").

In the present case, amended independent claim 59 recites limitations which distinctly claim the product for which protection is sought, that is an integrated circuit substrate formed as a result of a particular etching process, by "generating a plasma of said etching gas at a first power level" and "generating a plasma of said etching gas at a second power level . . . wherein said second power level plasma is a higher power plasma than said first power level plasma." Because claims 59-84 recite a resulting structure produced by using these particular etching parameters and which "cannot be adequately described in any other manner," the product-by-process claims 59-84 are "perfectly acceptable one(s)."

In addition, Summerfelt does not disclose the limitations of claims 59-65 and 67-84. Summerfelt is silent about an "integrated circuit substrate" formed by the steps recited in amended independent claim 59. As noted above, Summerfelt relates to high-dielectric constant capacitor electrodes and methods of improving the adhesion between oxygen-stable layers and these material electrodes, and not to an integrated circuit substrate formed by *inter alia* "generating a plasma of said etching gas at a first power level and

contacting said substrate with said first power level plasma for a first predetermined time" and "generating a plasma of said etching gas at a second power level in said chamber and contacting said integrated circuit substrate with said second power level plasma for a second predetermined time, wherein said second power level plasma is a higher power plasma than said first power level plasma," as amended independent claim 59 recites. For at least these reasons, Summerfelt fails to disclose all limitations of claims 59-65 and 67-84 and withdrawal of the rejection of these claims is respectfully requested.

Claims 59-61, 66 and 68-84 stand rejected under 35 U.S.C. § 102 as being anticipated by Harvey (U.S. Patent No. 6,057,227) ("Harvey"). This rejection is respectfully traversed.

Harvey relates to damascene structures and methods of formation. (Abstract). Harvey teaches "a damascene-formed structure which has interconnects with uniform depths" which is formed by "us[ing] a layer of non-stochiometric oxide dielectric as an etch stop." (Col. 3, lines 49-53). Harvey also teaches that "[A] layer of stochiometric oxide is then deposited over the etch stop layer." (Col. 3, lines 54-55).

Harvey does not disclose the limitations of claims 59-61, 66 and 68-84. Harvey is silent about an "integrated circuit substrate" formed by the method steps recited in amended independent claim 59. The crux of Harvey is the formation of "trenches which have uniform depths," and not achieving an integrated circuit substrate formed by a particular process methodology, as in the claimed invention. For at least these reasons, Harvey fails to disclose all limitations of claims 59-61, 66 and 68-84 and withdrawal of the rejection of these claims is respectfully requested.

New claims 92 and 93 have been added to round out the scope of protection afforded by the invention. The cited references fail to teach or suggest the subject matter of claims 92 and 93, including an "integrated circuit substrate formed by . . . (a) placing said integrated circuit substrate into a reactive chamber; (b) introducing an etching gas into said chamber" and "(c) generating a plasma of said etching gas at a first power level and contacting said substrate with said first power level plasma for a first predetermined time,"

as newly added claim 92 recites. The cited references also fail to teach or suggest "(d) generating a plasma of said etching gas at a second power level in said chamber and contacting said integrated circuit substrate with said second power level plasma for a second predetermined time, wherein said second power level plasma is a higher power plasma than said first power level plasma, and wherein said substrate has a CD loss decreased compared to the CD loss of a substrate formed by a method comprising said steps (a), (b) and (c) but not step (d)," as newly added claim 92 recites. The cited references further fail to teach or suggest that the CD loss is decreased "by about 400 Angstroms," as newly added claim 93 recites.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

By_____

Thomas J. D'Amico
Registration No.: 28,371
Gabriela Coman
Registration No.: 50,515
DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 785-9700
Attorneys for Applicant

VERSION WITH MARKINGS TO SHOW CHANGES MADE

59. (Amended) An integrated circuit substrate [having improved CD loss and reduced striations] formed by a method, comprising:

placing said integrated circuit substrate into a reactive chamber;

introducing into said chamber an etching gas;

generating a plasma of said etching gas at a first power level and contacting said substrate with said first power level plasma for a first predetermined time; and[,]

generating a plasma of said etching gas at a second power level in said chamber and contacting said integrated circuit substrate with said [high] second power level plasma for a second predetermined time, wherein said second power level plasma is a [high] higher power plasma [and is greater] than said first power level plasma[, which is a low power plasma].